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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/684,681	10/14/2003	Silvano Gai	112025-0181C1	3408
24267	7590	08/13/2004		
CESARI AND MCKENNA, LLP			EXAMINER	
88 BLACK FALCON AVENUE			COULTER, KENNETH R	
BOSTON, MA 02210			ART UNIT	PAPER NUMBER
			2141	

DATE MAILED: 08/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/684,681	GAI, SILVANO	
	Examiner Kenneth R Coulter	Art Unit 2141	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on \_\_\_\_\_.
- 2a) This action is **FINAL**.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 20-39 is/are pending in the application.
  - 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 20-39 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 14 October 2003 is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All    b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 10/30/03; 4/26/04.
- 4) Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: IDS: 4/30/04.

## DETAILED ACTION

### ***Double Patenting***

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 20 – 39 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 - 19 of U.S. Patent No. 6,658,458. Although the conflicting claims are not identical, they are not patentably distinct from each other because both the present Application and U.S. Pat. No. 6,658,458 disclose:

1. An information storage and searching device, the device comprising: a buffer for storing data to be searched, a barrel shifter (selector) operably controllable to select at least a portion of the buffer's contents; and a storage facility coupled to the barrel shifter so as to receive the selected portion of the buffer's contents, the storage facility having a plurality of associative memories arranged in a cascading fashion such that the output from an upstream associative memory is provided to at least one downstream associative memory, the associative memory being loaded with information against which data in the buffer is to be matched, wherein the information is translated into a Boolean function prior to

being loaded into the associative memories, and each associative memory stores a segment of the Boolean function.

2. The information storage and searching device of claim 1 further wherein the barrel shifter inputs a different portion of the buffer's contents into each associative memory.
3. The information storage and searching device of claim 2 further wherein each downstream associative memory compares its segment of information against the output from its respective upstream associative memory and the selected portion of the buffer's contents.
4. The information storage and searching device of claim 3 further wherein each associative memory has a plurality of entries, the storage facility further comprises a plurality of secondary memories each having a plurality of storage locations, and each secondary memory is associated with a corresponding associative memory such that each associative memory entry identifies a particular storage location of its associated secondary memory.
5. The information storage and searching device of claim 4 further wherein the Boolean function is a Binary Decision Diagram (BDD), and each associative memory stores a different BDD segment.
6. The information storage and searching device of claim 5 wherein each associative memory is a ternary content addressable memory (TCAM) supporting don't care values.
7. The information storage and searching device of claim 6 further comprising a controller operatively coupled to the barrel shifter, the controller configured to direct the barrel shifter to retrieve a selected portion of the buffer's contents.
8. The information storage and searching device of claim 7 wherein the information stored in the TCAMs corresponds to one or more access control lists (ACLs), and the data stored in the buffer corresponds to a network message.
9. An intermediate network device for use in processing and forwarding network messages in a computer network, the intermediate network device comprising: a plurality of ports for connecting the device to the computer network, each port configured to receive and forward network messages; a forwarding entity coupled to the ports for processing the network messages; and an information storage

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and searching device coupled to the forwarding entity for receiving one or more of the network messages, the information storage and searching device comprising: a buffer for storing the one or more network messages, means for selecting at least a portion of the buffer's contents; and a storage facility coupled to the selecting means so as to receive the selected portion of the buffer's contents, the storage facility having a plurality of associative memories arranged in a cascading fashion such that the output from an upstream associative memory is provided to a downstream associative memory, the associative memories being loaded with information against which data in the buffer is to be searched, wherein the information is translated into a Boolean function prior to being loaded into the associative memories, and each associative memory stores a segment of the Boolean function.

10. The intermediate network device of claim 9 wherein the selecting means of the information storage and searching device inputs a different portion of the buffer's contents into each associative memory.

11. The intermediate network device of claim 10 wherein the Boolean function is a Binary Decision Diagram (BDD), and each associative memory stores a different BDD segment.

12. The intermediate network device of claim 11 wherein the associative memories are ternary content addressable memory (TCAM) supporting don't care values.

13. A method of loading a storage facility having a plurality of associative memory stages with information to be matched, the method comprising the steps of: translating the information into a Binary Decision Diagram (BDD), the BDD having a plurality of nodes interconnected by arcs and one or more results; cutting the BDD into a plurality of segments such that the number of BDD segments corresponds to the number of associative memory stages in the storage facility; assigning a value to each BDD node reached by an arc crossing a cut; computing one or more coverages for each BDD segment such that the output of the coverage are either the values assigned to the BDD nodes in the next adjacent BDD segment or the results of the BDD; loading each associative memory stage with the one or more computed coverages for the respective BDD segment; and loading each associative memory stage with either the values assigned to the BDD nodes in the next adjacent BDD segment or the results of the BDD.

14. The method of claim 13 wherein the BDD includes a set of variables and each BDD segment includes a sub-set of the variables, and each computed

coverage has as its variables, the sub-set of variables from the corresponding BDD segment.

15. The method of claim 14 wherein each associative memory stage includes a corresponding secondary memory having a plurality of storage locations, and the values assigned to the BDD nodes reached by arcs crossing a cut and the results of the BDD are loaded into the storage locations of the secondary memories.

16. The method of claim 15 wherein the associative memories are ternary content addressable memory (TCAM) supporting don't care values.

17. The method of claim 16 wherein the information stored in the TCAMs corresponds to one or more access control lists (ACLs), and the data being matched against the contents of the TCAMs corresponds to a network message.

18. A computer readable medium containing executable program instructions for loading a storage facility having a plurality of associative memory stages with information to be matched, the executable program instructions comprising steps for: loading a storage facility having a plurality of associative memory stages with information to be matched, the method comprising the steps of: translating the information into a Binary Decision Diagram (BDD), the BDD having a plurality of nodes interconnected by arcs and one or more results; cutting the BDD into a plurality of segments such that the number of BDD segments corresponds to the number of associative memory stages in the storage facility; assigning a value to each BDD node reached by an arc crossing a cut; computing one or more coverages for each BDD segment such that the output of the coverage are either the values assigned to the BDD nodes in the next adjacent BDD segment or the results of the BDD; loading each associative memory stage with the one or more computed coverages for the respective BDD segment; and loading each associative memory stage with either the values assigned to the BDD nodes in the next adjacent BDD segment or the results of the BDD.

19. The computer readable medium of claim 18 wherein each BDD segment includes a plurality of variables and the one or more coverages for a given BDD segment has as inputs the values assigned to the BDD nodes within the given BDD segment that are reached by arcs from the previous BDD segment, and the variables within the given BDD segment.

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3. However, U.S. Pat. No. 6,658,458 does not explicitly disclose **pre-parser logic** configured to extract one or more fields of a network message.

U.S. Pat. No. 6,658,458 discloses an equivalent barrel shifter that selects at least a portion of the buffer's contents.

4. However, U.S. Pat. No. 6,658,458 does not explicitly disclose that the network message is an **Internet Protocol Version 6 (Ipv6)** message.

The Examiner hereby takes official notice that Ipv6 messages are commonplace in the art and therefore represent no patentably distinct feature over the prior art of record.

5. In addition, U.S. Pat. No. 6,658,458 does not explicitly disclose that each segment of the BDD is translated into a **Sum of Products (SOP)** format prior to being loaded into its respective memory.

The Examiner hereby takes official notice that the translation of information into a second Boolean representation such as SOP from a first Boolean representation is commonplace in the art.

6. In addition, U.S. Pat. No. 6,658,458 does not explicitly disclose that the information searching device of claim 20 is formed from:

- (a) one or more **Application Specific Integrated Circuits (ASICs)**;
- (b) one or more **Field Programmable Gate Arrays (FPGAs)**; or
- (c) at least one ASIC or at least one FPGA.

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The Examiner hereby takes official notice that these circuitry specifics are notoriously commonplace in the art and therefore represent no patentably distinct feature over the prior art of record.

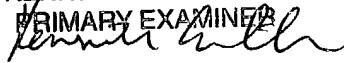
7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth R Coulter whose telephone number is 703 305-8447. The examiner can normally be reached on 549.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rupal Dharia can be reached on 703 305-4003. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KENNETH R. COULTER

PRIMARY EXAMINER



krc